executing a timing analysis to the layout by using the delay times calculated by the delay time calculator--.

Claim 20 line 1 after "product"; insert **–stored on a computer-readable medium--.**

Claim 20 line 5 after " designed;" delete " and".

Claim 20 line 5 after "designed"; insert --;

instructions configured to calculate delay times of the low-threshold cells in state that the upper limit electric potential of the virtual ground line is set--.

Claim ~~1~~ 20 lines ~~8~~ 9 after "cells"; insert --; **and** KW 3/6/07

instructions configured to execute a timing analysis to the layout by using the delay times calculated by the delay time calculator--.

Reasons for Allowance

The following is an examiner's statement of reasons for allowance:

2. Claims 1-20 are allowed because the prior art does not teach or suggest: an automatic circuit design apparatus comprising: a delay time calculator configured to calculate delay times of the low-threshold cells in state that the upper limit electric potential of the virtual ground line is set; a layout generator configured to generate a layout such that an electric potential of the virtual ground line does not exceed the upper limit electric potential, the layout generated based on the information, the cell library for low-threshold cells, and the cell library for high-threshold cells; and a timing analyzer configured to execute a timing analysis to the layout by using the delay times calculated by the delay time calculator and combination of all other features corresponding to the independent claims.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".